Thesis Summary

This document summarises the Master's thesis titled *PCB Component Placement using Reinforcement Learning (RL)*. First, the topic is introduced with a brief motivation and problem description. Next, the literature review outcomes are described before investigating state-of-the-art approaches. Lastly, our novel placement methodology and an accompanying solution are presented.

Printed Circuit Boards (PCBs) are at the centre of all electronic systems and provide the surface onto which electronic components are soldered and the routing infrastructure for wiring them together. They are three-dimensional structures with many internal copper layers along which wires are etched spanning both horizontally and vertically. The PCB design process involves translating the logical topology of a circuit (e.g. a schematic) into a manufacturable geometrical representation and is divided into component placement followed by routing. Automated placement techniques have had some success [1, 2], but they often lack the intuitive understanding of human engineers. Partly for this reason, such tools did not gain traction, and presently it is a predominantly manual process. The thesis investigates the current state-of-the-art [3] and proposes a novel end-to-end machine-learning approach to optimise the placement of components on a PCB. We aim to create an AI-assisted workflow that enhances productivity by allowing designers to focus on higher-level tasks, reducing design time while leveraging the differentiating benefits of customised solutions.

The placement task accepts a circuit netlist describing the logical representation of the circuit accompanied by geometrical information of the individual components (e.g. dimensions) [4]. The task is at least NP-Complete [5] and is concerned with identifying the best spatial location and orientation for all the components given solution constraints (e.g. no overlaps) and optimisation goals (e.g. minimised wirelength) [6]. Placement techniques can be classified as constructive and iterative. The former order the circuit netlist according to a criterion (e.g. component area) and sequentially place the constituents onto an empty layout region. The latter starts with a randomly initialised placement that is iteratively improved until a terminal condition is reached.

PCB and Integrated Circuit (IC) placement processes share many commonalities, but problem size is one aspect they greatly differ. As a result, research on the former is sparse [7, 8] and limited primarily to particular placement co-optimisation tasks [9-12]. By contrast, since IC (digital) design is only feasible with automated tools, it has a thriving research community with contributions from academia [14-19] and industry [20-23]. Since the 1960s, four placement categories have emerged, namely, partitioning-based methods inspired by graph theory [24, 25], black-box optimisation methods [2, 26-29], analytic placement [16, 17, 30-38] and presently, learning-based solutions [3, 39, 40]. Metaheuristics proved effective while offering flexibility in defining the objective function. However, driven by stochastic decision processes, they were not feasible on circuits exceeding 1e5 elements. Analytic placement appeared as a more scalable alternative and is presently considered state-of-the-art [14, 15, 22]. It requires a differentiable objective that is optimised using numerical techniques. Recently hybrid [39, 40] and end-to-end solutions [3] for floorplanning using RL have been proposed, albeit they are still in their infancy. RL offers attractive solutions to such problems, particularly for its ability to represent vast state spaces and generalise to unseen similar ones.

The thesis initially investigates the state-of-the-art constructive placement methodology by Mirhoseini et al. [3] and proposes a novel formulation for iterative placement. Mirhoseini et al. proposed using a neural network to represent the problem state in a compressed manner. They offer a novel edge-based graph neural network to automatically extract features from the circuit netlist and, together with task-relevant metadata, they predict a placement quality metric as a linear combination of wirelength, congestion and density. After removing the final prediction layer, the authors encoded the problem state and used PPO [48] to train RL policies for predicting placement probabilities over a discretised layout region. Using this approach as a guideline, we trained a neural network to predict circuit wirelength and subsequently trained policies using TRPO [47] and PPO in a similar way. Using unseen circuits, we achieved an accuracy of 69.5% for the graph-level wirelength prediction task, albeit subsequent RL policies were significantly outperformed by 41% after establishing a baseline with Simulated Annealing (SA) [42, 43]. While the authors provided innovative ideas, we were concerned about important details as well as their evaluation procedures. Recent literature shared similar concerns [40] and even debunked some of the original claims [50].

Learning from the previous limitations, we formulated the iterative PCB placement task as a Markov Decision Process (MDP). First, we studied its mechanics in a constrained environment (single-component approach), then pooled our findings and adapted the setup to yield general solutions (multi-component approach). Concerning the former, the agent represents a single component. The goal, starting from an arbitrary location on the PCB, is to orient the component within a fixed optimised layout while minimising wirelength and avoiding overlap in the terminal state. The observation space mainly captures the perceived surroundings and direction information related to movement. We propose two fundamentally distinct reward signals to motivate the desired behaviour. First, we attempt to mimic the expert by using expert positioning as the goal. Secondly, we motivate self-improvement using problem-related performance metrics. We extensively study the problem by investigating a variety of RL algorithms [46-50], discrete and continuous action spaces, and environment features such as optimal episode length, step size and replay buffer size, especially in cases of adaptive reward signals. Our overarching aim was to learn fundamental placement techniques applicable to unseen circuits. While we learned a lot from these experiments, we concluded that expert-generated data introduce inconsistencies that prevent generalisation. These inconsistencies leaked into our problem setup through the reward signal when mimicking the expert and through the observation space arising from the fixed portion of the circuit.

To address data inconsistencies, we adapted the training process to suit a multi-component setup that simultaneously places all components except one. In other words, we lock a single component to serve as an anchor (typically the main IC) and for every step in the episode, we invoke the policy on all the moveable components (all except the anchor), each time sampling an updated environment state. This training process collects highly diverse data points because every component in the circuit contributes a different perspective into the problem. In pursuit of generalisation, we use a dataset of nine circuits sampled from real-world applications having up to 12 components. We train on six and evaluate on the remaining three. We establish a baseline using SA [42, 43] and compare placements in terms of post-routing wirelength [44] after 600 iterations. For each circuit, we average four evaluations starting from different conditions. Over the three unseen circuits, our best configuration outperforms SA by up to 21%. Additionally, we observed that optimised placements generated by our method can converge over an order of magnitude faster, suggesting that leveraging experience over stochastic decision-making is beneficial. Quantitatively the policies exhibit fundamental placement techniques (i.e. witnessed taking actions to minimise wirelength) and emergent collaborative or competitive features conditional on the reward scheme.

The thesis proposed a novel MDP formulation for iterative placement and delivered a general RL solution. Although further optimisations and additional key features are necessary, this work offers a promising direction towards automating PCB component placement. A demonstration is available on GitHub, while the complete thesis and associated publication are available on my website.

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